

Appl. No.: 09/540,952  
Amdt. dated August 11, 2003  
Reply to Office action of April 9, 2003

### REMARKS

Applicants appreciate the Examiner's detailed Office Action and consideration of Applicants' claimed invention.

Applicants have amended the application as shown above to correct clerical errors and to clarify the claims and specification where appropriate.

In ¶ 2, the Office Action objects to Claims 5, 18 and 31 as duplicative of Claims 2, 15, and 28. Accordingly, Applicants have cancelled Claims 5, 18 and 31.

With respect to all pending claims, Claims 1-4, 6-17, 19-30, and 32-39, Applicants respectfully submit that these claims are allowable for at least the reasons set forth below:

**I. Rejection Under 102(e):**

In ¶ 2, the Office Action rejects all pending claims, Claims 1-39, under 102(e) as being anticipated by Levine et al., U.S. Pat. No. 6,134,710. In particular, the Office Action rejects Claim 1 (and the other independent claims) of the patent submitting in part that the Levine reference discloses the claimed limitation of "determining a latency associated with a particular object code instruction ... the particular object code instruction being executed by the computer...". Specifically, the Office Action references col. 8, lines 4-17 in which Levine references monitoring "stalls and durations". Levine at col. 8, line 7. Applicants respectfully disagree that Levine teaches the claimed elements of Applicants' invention.

As amended, Claim 1 recites in part **"determining a latency of a particular object code instruction ... the particular object code instruction being executed by the computer ...."** Levine fails to teach this limitation.

Levine discloses a system and method to monitor the performance of a computer processing system when executing an application program. Levine at col. 1, lines 6-12. The system profiles instances of operational segments of the program such as long table walks and cache misses, analyzes the profiled data, and modifies the object code on-line in order to improve the operation of the application program in the processing system. Levine at col. 1, lines 6-12.

Appl. No.: 09/540,952  
Amdt. dated August 11, 2003  
Reply to Office action of April 9, 2003

While Levine may contemplate monitoring the number of stalls and delays as indicated in the portion of Levine cited in the Office Action, Levine does not actually **"determine a latency of a particular object code instruction"** as recited in the claims. Instead, Levine simply monitors where and when delays (such as long table walks and cache misses) occur to identify the offending instructions and to implement remedial preload instructions. Instead of determining the latency of a particular instruction, Levine just monitors events such as data cache misses that exceed a specified threshold. See e.g., *Levine at col. 10, lines 59-67 (interrupt signaled when predetermined number of cache misses that exceed a specific threshold value of time, as determined by MMCR0 110 and thresholder 180)*. In short, Levine does not determine a latency of an instruction, but uses a threshold of time to identify when particular events or instructions exceed that threshold. See *Levine at col. 8, lines 39-44*.

The fact that Levine does not **"determine a latency of a particular object code instruction"** is made particularly clear when Levine contemplates where to insert preload instructions to help remediate delays of offending instructions, such as instructions causing long data cache misses.

The preload instruction should be positioned before the offending instruction by at least a time interval that is equivalent to the threshold value used to determine long cache misses. By using the number of processor cycles that is equivalent to the threshold value, and by using the average number of processor cycles per instruction, the number of instructions equivalent to the threshold value may be determined. *Levine at col. 12, lines 50-58*.

Thus, Levine does not use a determined latency of a particular offending instruction. Rather, Levine can only use the fact that the delay of the offending instruction was at least the threshold value used to identify such offending instruction.

Ultimately, Levine is not directed to determining the latency of a particular object code instruction. Accordingly, for at least all of the foregoing reasons, independent claims 1, 14, and 27 (and all claims depending therefrom) are allowable over Levine.

Appl. No.: 09/540,952  
Amdt. dated August 11, 2003  
Reply to Office action of April 9, 2003

**II. Rejection Under 103(a):**

The Office Action also rejects Claims 11-13, 24-26, and 37-39 under 35 U.S.C. 103(a) as being unpatentable over Levine in view of Krishnaswamy, U.S. Pat. No. 6,308,318. In particular, the Office Action submits that Levine discloses all the claimed limitations of Claim 1. See *Office Action* p. 5. The Office Action acknowledges, however, that Levine does not teach "interpreting the instructions of the at least one issue block and wherein said particular object code instruction is in the issue block." *Id.* The Office Action submits that Krishnaswamy does disclose this feature. *Id.* (citing col. 5, lines 45-55). Applicants respectfully disagree that the combination of Levine and Krishnaswamy disclose or make obvious the invention as claimed by Applicants.

First, the Office Action has made no prima facie showing of why it would be appropriate to combine these references or why there would be a reasonable expectation of success if the references were combined. See *MPEP* 2143. The Office Action presents no suggestion in either of the references that would suggest combining the references nor that such a combination would likely be successful. Accordingly, Applicants respectfully submit that without such a showing of prima facie obviousness, the rejection cannot stand.

Second, even if the references are combined, however, Levine does not teach or suggest the limitations in the independent claims (See remarks above: Rejection Under 102(e)). In addition, Krishnaswamy does not disclose or teach anything related to **determining a latency of a particular object code instruction** as is claimed by Applicants. For at least these reasons, the claims are allowable over the combination of Levine and Krishnaswamy.

**III. Conclusion**

Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a

OFFICIAL

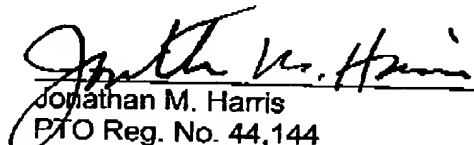
Appl. No.: 09/540,952  
Amdt. dated August 11, 2003  
Reply to Office action of April 9, 2003

particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

  
Jonathan M. Harris  
PTO Reg. No. 44,144  
CONLEY ROSE, P.C.  
(713) 238-8000 (Phone)  
(713) 238-8008 (Fax)  
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
Legal Dept., M/S 35  
P.O. Box 272400  
Fort Collins, CO 80527-2400